IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant | : Eitan Rosen | Art Unit | : 2116 |
| Serial No. | : 10/631,327 | Examiner | : Tse W. Chen |
| Filed | : July 30, 2003 | Conf. No. | : 1395 |
| Title | : DDR INTERFACE BUS CONTROL | | |

**Mail Stop Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

This brief is filed in response to factual deficiencies in the Final Office Action mailed April 20, 2007 and Advisory Action mailed August 30, 2007. Claims 1-15 and 23-37 are pending in the action, with claims 1 and 23 being independent.

**Section 102(b) Rejections**

Claims 1, 3, 5-6, 11-14, 23-25, 27-28 and 33-36 are rejected as being anticipated by Anzai. Claim 1 recites in part a driver in communication with a clock bus, the driver to drive and maintain a voltage of the clock bus to a first voltage level **while** a clock transmitter is not transmitting a clock signal on the clock bus and a clock receiver is not receiving a clock signal on the clock bus.

In the Final Office Action, the Examiner maintains that Anzai's output circuit 109 corresponds to Applicant's claimed driver, and that Anzai's transfer clock 'c' (signal (L) in Fig. 5) corresponds to Applicant's claimed clock bus. *See*, page 2, item 3 of Office Action.

Anzai describes a data transfer system for improving data transfer speed in serial transmission.

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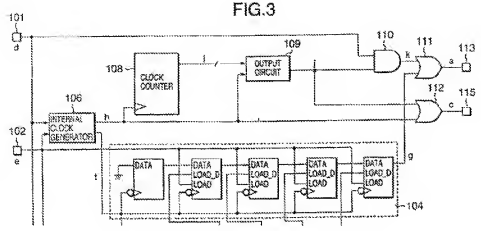
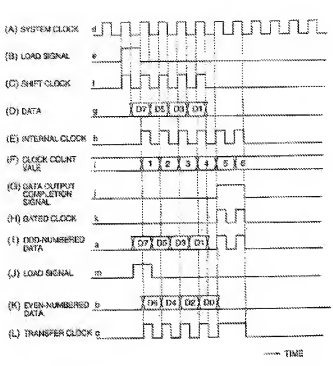
FIG.3




As shown in the figure above, Anzai's clock counter 108 generates a clock count value 'i', which is output to the output circuit 109. The output circuit 109 decodes the clock count value 'i' using the internal clock signal 'h' from the internal generator 106 to produce a data output completion signal 'j' (7:27-31). Anzai's system transfers 8-bit data during a period equal to six clock pulses of the transfer clock 'c' (5:66-67). When the clock count reaches a value of six, indicating that the last bit of the 8-bit serial data has been transmitted, the output circuit generates a completion signal 'j' (7:26-30 & 5:52-54). Anzai's OR circuit 112 then performs an OR operation on the completion signal 'j' and the internal clock signal 'h' to generate the transfer clock signal 'c' (6:35-37). As shown in Figs. 2 and 5, the OR operation causes the transfer clock signal 'c' to go high "during a period from the leading edge to the trailing edge of the odd-numbered data" (2:28-31, 5:44-46 & 5:59-62). After this period (i.e., after the completion signal 'j' terminates) the transfer clock signal 'c' floats low (Fig 5). Anzai's sending unit 100 transmits the transfer clock signal 'c' via the output terminal 115 to input 203 of Anzai's receiving unit (6:36-37 & 6:43-45).

Applicant respectfully asserts that Anzai fails to teach or suggest, at least, a driver to drive and maintain a voltage of the clock bus to a first voltage level while the clock transmitter is not transmitting a clock signal on the clock bus. The Examiner suggests that Anzai's transfer clock signal 'c' is maintained LOW after completion signal 'j' terminates. See, page 2, item 3 of Office Action. Applicant respectfully disagrees, and submits that Anzai's transfer clock signal 'c' is maintained at *two different levels* after data transmission completes.




As shown in Fig. 5 above, the transfer clock signal 'c' is held HIGH for the duration of the completion signal 'j', and is held LOW after the completion signal 'j' terminates (5:59-65). Applicant respectfully asserts that Anzai's HIGH state of the transfer clock signal 'c' is not Applicant's claimed first voltage level, and Anzai does not drive or maintain this state while the clock transmitter is not transmitting a clock signal on the clock bus. By contrast, Anzai''s clock transmitter 100 is transmitting clock signals during this state: the system clock 'd' is continuously transmitting, and the internal clock generator 106 continuously transmits the internal clock 'h' until the falling edge of transfer clock signal 'c'. (Fig. 5).

Similarly, the floating state of transfer clock signal 'c' is not Applicant's claimed first voltage level. After the completion signal 'j' terminates, transfer clock signal 'c' transitions to LOW and remains floating. Anzai does not provide any teaching or suggestion that the clock signal 'c' is maintained at *any* particular voltage level.

Applicant respectfully submits that the transfer clock signal 'c' is not driven and maintained to a first voltage level when Anzai is viewed in its entirety. As discussed above, transfer clock signal 'c' is held at multiple levels, i.e., a high state and a low floating state. In fact, Anzai's design *requires* these multiple levels, because it is the high-to-low transition that

indicates to the receiving unit 200 that data transmission is complete (5:62-65 & 7:38-44). Because Anzai's output circuit maintains the transfer clock at not one, but *two* different voltage levels, Applicant respectfully submits that Anzai does not anticipate claim 1 for at least these reasons.

The Examiner also argues that "claim 1 does not indicate when the maintaining of the voltage of the clock bus to a first voltage level begins" but requires only "the maintaining of the voltage of the clock bus in reference to a first voltage level". *See*, page 7, lines 18-22 and page 8, lines 1-4 of Final Office Action.

Applicant respectfully disagrees with this characterization of claim 1. Claim 1 specifically recites a driver to drive and maintain a voltage of the clock bus to a first voltage level **while** a clock transmitter is not transmitting a clock signal on the clock bus and a clock receiver is not receiving a clock signal on the clock bus. As defined by Merriam-Webster online dictionary (see Exhibit "A"), the term "while" is defined as "a period of time especially when short and marked by the occurrence of an action". Based on this definition, Applicant respectfully submits that claim 1 readily sets forth when the maintaining of the voltage of the clock bus to a first voltage level commences: the period of time during which "the clock transmitter is not transmitting a clock signal on the clock bus and a clock receiver is not receiving a clock signal on the clock bus" (i.e., the occurrence of an action). Anzai provides no teaching for driving and maintaining the transfer clock 'c' at any voltage level during such period. For at least these reasons, Applicant respectfully submits that Anzai does not anticipate claim 1.

**Claim 23**

Claim 23 also recites a voltage driving means for driving and maintaining a voltage of a clock bus to a first voltage level **while** a clock signal transmission means is not transmitting a clock signal on the clock bus and a clock signal receiving means is not receiving a clock signal on the clock bus.

As discussed above, Anzai does not teach or suggest at least these functions or the means for performing such. For at least the reasons discussed with respect to amended claim 1, Applicant respectfully submits that Anzai does not anticipate claim 23 and that claim 23 is

therefore allowable. Claims 24-37 depend on claim 23, and also are submitted to be allowable for at least reasons discussed with respect to claim 23.

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Respectfully submitted,

Date: September 20, 2007

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